ABSTRACT

The object of the present invention is to reduce, in the fabrication of a semiconductor device with a multi-layered interconnection, stresses imposed on conductive elements by interlayer dielectric films made of different materials.

For a given multi-layered semiconductor device in which a test conductive element is flanked by plural interlayer dielectric films made of different materials, stresses imposed on the test conductive element by the interlayer dielectric films are determined by calculation. The calculation is based on an equation involving an average thermal expansion coefficient of the dielectric films which is obtained from the thermal expansion coefficients of individual dielectric films and their relative volumes, the temperature at which a conductive material constituting the test conductive element undergoes stress relaxation, and the highest observable temperature during fabrication. Maximum temperature to be observed during fabrication and the materials and relative thicknesses of individual dielectric films are appropriately adjusted such that the stress value obtained by calculation is below a specified tolerable level which is known to cause no void formation around the test conductive element.